Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An integrated circuit comprising:

one or more functional blocks to be tested when said integrated circuit is placed in a test mode;

one or more test structures configured to test said one or more functional blocks when said integrated circuit is placed in said test mode;

a wireless interface which receives ~~said~~ test data over a wireless connection, the test data comprising a frame having a plurality of bits; and

a test access mechanism which controls input of said received test data to said test structures, wherein at least two of said plurality of bits of the frame are applied to different respective test structures on said integrated circuit.

2. (Original) An integrated circuit in accordance with claim 1, wherein:

said wireless interface implements an Internet Protocol stack which extracts test data from, and transmits test results over, said wireless connection in formatted frames.

3. (Canceled)

4. (Original) An integrated circuit in accordance with claim 1, wherein:

said test structures comprise one or more scan chains; and

said test access mechanism comprises a scan chain loading mechanism.

5. (Currently Amended) An integrated circuit in accordance with claim 4, wherein:

said scan chain loading mechanism simultaneously loads a plurality of scan chains with different bits of the frame of said test data.

6. (Currently Amended) An integrated circuit in accordance with claim 4, wherein:

the different bits of the frame are loaded into the ~~said scan chain loading mechanism loads~~ one or more scan chains in parallel.

7. (Currently Amended) A system for testing an integrated circuit, comprising:

~~a test station comprising:~~

~~a wireless interface which receives test data for said integrated circuit and transmits said test data over a wireless connection; and~~

~~one or more respective~~ a plurality of integrated circuits, each comprising:

one or more functional blocks to be tested when said integrated circuit is placed in a test mode;

one or more test structures configured to test said one or more functional blocks when said integrated circuit is placed in said test mode;

a wireless interface which receives and extracts ~~said~~ test data from a wireless connection; and

a test access mechanism which controls input of said received test data to said test structures; and

a test station comprising a test station wireless interface which simultaneously transmits the test data over the wireless connection to the wireless interfaces of each of the plurality of integrated circuits.

8. (Currently Amended) A system in accordance with claim 7, wherein:

each of the wireless interfaces of the plurality of integrated circuits ~~said wireless interface~~ implements an Internet Protocol stack which extracts test data from, and transmits test results over, said wireless connection in formatted frames.

9. (Currently Amended) A system in accordance with claim 8, wherein:

said test data comprises a frame ~~comprising one or more bytes, words, or blocks and corresponding bits of said one or more bytes, words, or blocks comprise test data for driving~~ having a plurality of bits at least two of which are driven to respective different test structures on said respective one or more integrated circuits.

10. (Currently Amended) A system in accordance with claim 7, wherein:

said test structures on said ~~one or more~~ respective plurality of integrated circuits comprise one or more scan chains; and

said test access mechanism on said ~~one or more~~ respective plurality of integrated circuits comprises a scan chain loading mechanism.

11. (Currently Amended) A system in accordance with claim 10, wherein:

said scan chain loading mechanism on ~~said one or more~~ each of said respective plurality of integrated circuits simultaneously loads a plurality of scan chains.

12. (Currently Amended) A system in accordance with claim 10, wherein:

said scan chain loading mechanism on ~~said one or more~~ each of said respective plurality of integrated circuits loads one or more scan chains in parallel.

13. (Currently Amended) A method for testing integrated circuits ~~an integrated circuit~~, comprising:

obtaining test data;

simultaneously sending said test data via a wireless interface over a wireless connection to ~~one or more respective device under tests~~ a plurality of integrated circuit devices under test, each ~~said one or more respective device under tests~~ comprising one or more functional blocks to be tested when said respective integrated circuit device under test is placed in a test mode, one or more test structures configured to test said one or more functional blocks when

said respective integrated circuit device under test is placed in said test mode, a wireless interface which receives and extracts said test data from said wireless connection; and a test access mechanism which controls input of said received test data to said test structures of said respective integrated circuit device under test.

14. (Currently Amended) A method in accordance with claim 13, comprising:

receiving test results via said wireless interface from said wireless connection from said ~~one or more respective device under tests~~ plurality of integrated circuit devices under test, said test results returned from said one or more test structures of said ~~one or more respective device under tests~~ respective plurality of integrated circuit devices under test from application of said test data to said one or more functional blocks of said respective pl of integrated circuit devices under test.